REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R195-94.	94-06-01	M. A. FRYE
B	Update drawing to reflect current requirements. -rrp	02-04-11	R. MONNIN

REV																				
SHEET																				
REV	B																			
SHEET	15																			
REV STATUS				REV			B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Dan Wonnell

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS

AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Sandra Rooney

APPROVED BY
Michael A. Frye

MICROCIRCUIT, LINEAR, A/D CONVERTER, 12-BIT, CMOS, MONOLITHIC SILICON

DRAWING APPROVAL DATE
94-02-17

REVISION LEVEL	SIZE	CAGE CODE	
B	A	**67268**	**5962-93179**

SHEET 1 OF 15

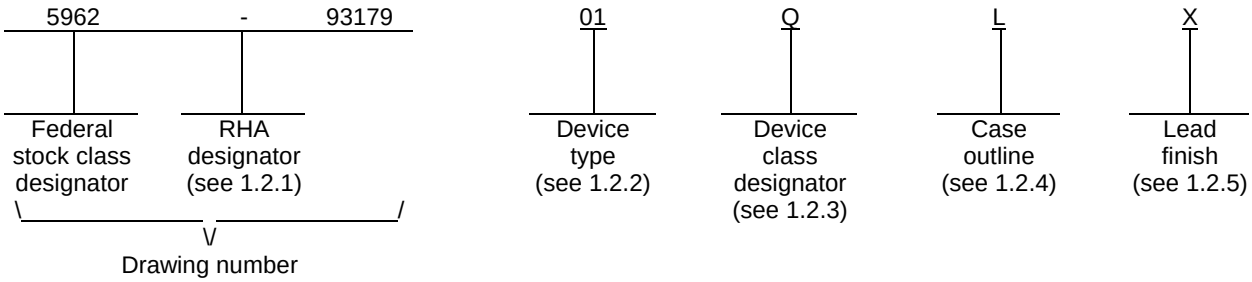
DSCC FORM 2233
APR 97

5962-E336-02

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD7876TQ	12-bit A/D converter with track/hold

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

V_{DD} to AGND	-0.3 V dc to +7.0 V dc
V_{SS} to AGND	+0.3 V dc to –7.0 V dc
AGND to DGND	-0.3 V dc to V_{DD} + 0.3 V dc
V_{IN} to AGND	-15 V dc to +15 V dc
REF_{OUT} to AGND	0 V dc to V_{DD}
Digital inputs to DGND	-0.3 V dc to V_{DD} + 0.3 V dc
Digital outputs to DGND	-0.3 V dc to V_{DD} + 0.3 V dc
Power dissipation at T_A = +75°C (P_D) 2/	450 mW
Lead temperature (soldering, 10 seconds)	+300°C
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Positive supply voltage (V_{DD})	+4.75 V dc to +5.25 V dc
Negative supply voltage (V_{SS})	-4.75 V dc to –5.25 V dc
AGND	0 V dc
DGND	0 V dc
External clock frequency (f_{CLK})	2.5 MHz
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Derate linearly at 10 mW/°C above T_A = +75°C.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 81 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution	RES		1,2,3	All	12		Bits
Integral nonlinearity	INL		1,2,3	All		±1.0	LSB
Differential nonlinearity	DNL		1,2,3	All		±1.0	LSB
Bipolar zero error	BZE		1,2,3	All		±6.0	LSB
Full scale error	FSE	2/	1	All		±8.0	LSB
			2,3			±30	
Track/hold acquisition time	T_{ACQ}	3/	9,10,11	All		2.0	µs
Analog input voltage range	V_{IN}		1,2,3	All		±10	V
Analog input current	I_{IN}		1,2,3	All		±600	µA
REF_{OUT} voltage	V_{REF}		1	All	2.99	3.01	V
REF_{OUT} voltage temperature coefficient	$\Delta V_{REF}/\Delta T$		2,3	All		±60	ppm/°C
REF_{OUT} voltage load sensitivity	$\Delta V_{REF}/\Delta I$	Reference load current change = 0 to 50 µA 4/	1,2,3	All		-1.0	mV
Input logic high voltage	V_{INH}	3/	1,2,3	All	2.4		V
Input logic low voltage	V_{INL}	3/	1,2,3	All		0.8	V
Output logic high voltage	V_{OH}	I_{SOURCE} = 40 µA	1,2,3	All	4.0		V
Output logic low voltage	V_{OL}	I_{SINK} = 1.6 mA	1,2,3	All		0.4	V
Input current	I_{IN}	V_{IN} = 0 V to V_{DD}	1,2,3	All		±10	µA
		12/$\overline{8}$ /CLK input only, $V_{IN} = V_{SS}$ to V_{DD}				±10	
Supply current	I_{DD}		1,2,3	All		13	mA
	I_{SS}					6.0	
Input capacitance	C_{IN}	See 4.4.1c	4	All		10	pF
DB11 – DB0 floating state output capacitance	C_{OUT}	See 4.4.1c	4	All		15	pF
DB11 – DB0 floating state leakage current	I_L		1,2,3	All		10	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
External clock conversion time	t_{CONV} (ext)	f_{CLK} = 2.5 MHz, see figure 2	9,10,11	All	7.2	8.0	µs
Internal clock conversion time	t_{CONV} (int)	See figure 2	9,10,11	All	6.5	9.0	µs
$\overline{CONVST}$ pulse width	t_1	5/ 6/	9	All	50		ns
$\overline{CS}$ to $\overline{RD}$ setup time (mode 1)	t_2	5/ 6/	9	All	0		ns
$\overline{RD}$ pulse width	t_3	5/	9,10,11	All	75		ns
$\overline{CS}$ to $\overline{RD}$ hold time (mode 1)	t_4	5/ 6/	9	All	0		ns
$\overline{RD}$ to $\overline{INT}$ delay time	t_5	5/ 6/	9	All		70	ns
Data access time after $\overline{RD}$	t_6	5/ 7/	9,10,11	All		70	ns
Bus relinquish time after $\overline{RD}$	t_7	5/ 8/	9,10,11	All	5.0	50	ns
HBEN to $\overline{RD}$ setup time	t_8	5/ 6/	9	All	0		ns
HBEN to $\overline{RD}$ hold time	t_9	5/ 6/	9	All	0		ns
$\overline{SSTRB}$ to SCLK falling edge setup time	t_{10}	5/ 6/	9	All	100		ns
SCLK cycle time	t_{11}	5/ 6/ 9/	9	All	370		ns
SCLK to valid data delay time	t_{12}	5/ 6/ 10/	9	All		150	ns
SCLK rising edge to $\overline{SSTRB}$	t_{13}	5/ 6/	9	All	20	100	ns
Bus relinquish time after SCLK	t_{14}	5/ 6/	9	All	10	100	ns
$\overline{CS}$ to $\overline{RD}$ setup time (mode 2)	t_{15}	5/ 6/	9	All	60		ns
Propagation delay time, $\overline{CS}$ to $\overline{BUSY}$	t_{16}	5/ 6/	9	All		120	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data setup time prior to $\overline{BUSY}$	t_{17}	5/ 6/	9	All	200		ns
$\overline{CS}$ to $\overline{RD}$ hold time (mode 2)	t_{18}	5/ 6/	9	All	0		ns
HBEN to $\overline{CS}$ setup time	t_{19}	5/ 6/	9	All	0		ns
HBEN to $\overline{CS}$ setup time	t_{20}	5/ 6/	9	All	0		ns

1/ V_{DD} = +4.75 V to +5.25 V, V_{SS} = -4.75 V to –5.25 V, AGND = DGND = 0 V, f_{CLK} = 2.5 MHz external.

2/ Includes internal reference error and is calculated after bipolar zero error has been adjusted out.

3/ Guaranteed by dc accuracy test results when used as a setup condition.

4/ Reference load should not be changed during conversion.

5/ Input t_r , t_f = 5.0 ns (10% to 90% of +5.0 V), timing voltage reference level = 1.6 V, see figure 2.

6/ Guaranteed if not tested.

7/ Test t_6 is defined as the time required for an output to cross 0.8 V or 2.4 V.

8/ Test t_7 is defined as the time required for the data lines to change 0.5 V.

9/ SCLK mark/space ratio (measured from a voltage level of 1.6 V) is 40/60 to 60/40.

10/ SDATA will drive higher capacitive loads but will add to t_{12} since it increases the external RC time constant (4.7 kΩ || C_L) and hence the time to reach 2.4 V, C_L = 35 pF.

Device type	01
Case outline	L
Terminal number	Terminal symbol
1	$\overline{RD}$
2	$\overline{BUSY}$ / $\overline{INT}$
3	CLK
4	DB11/ $\overline{HBEN}$
5	DB10/ $\overline{SSTRB}$
6	DB9/SCLK
7	DB8/SDATA
8	DB7/Low
9	DB6/Low
10	DB5/Low
11	DB4/Low
12	DGND
13	DB3/DB11
14	DB2/DB10
15	DB1/DB9
16	DB0/DB8
17	V_{DD}
18	AGND
19	REF_{OUT}
20	V_{IN}
21	V_{SS}
22	12/ $\overline{8}$ /CLK
23	$\overline{CONVST}$
24	$\overline{CS}$

FIGURE 1. Terminal connections.

Mode 1, 12-bit parallel read

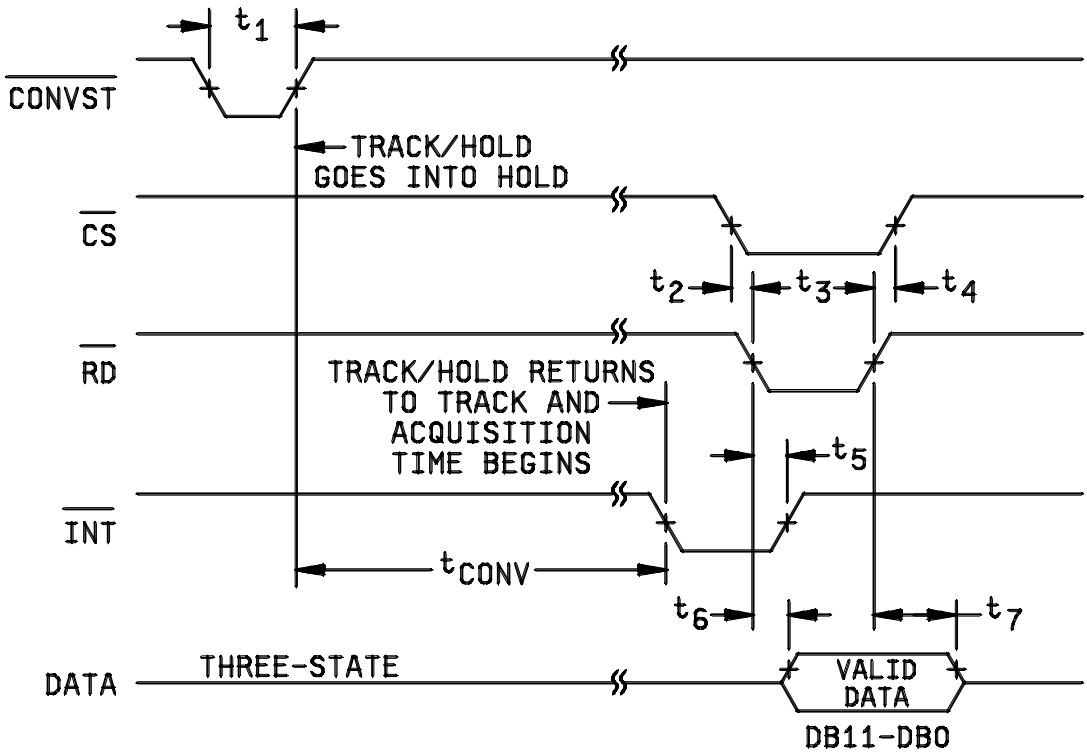
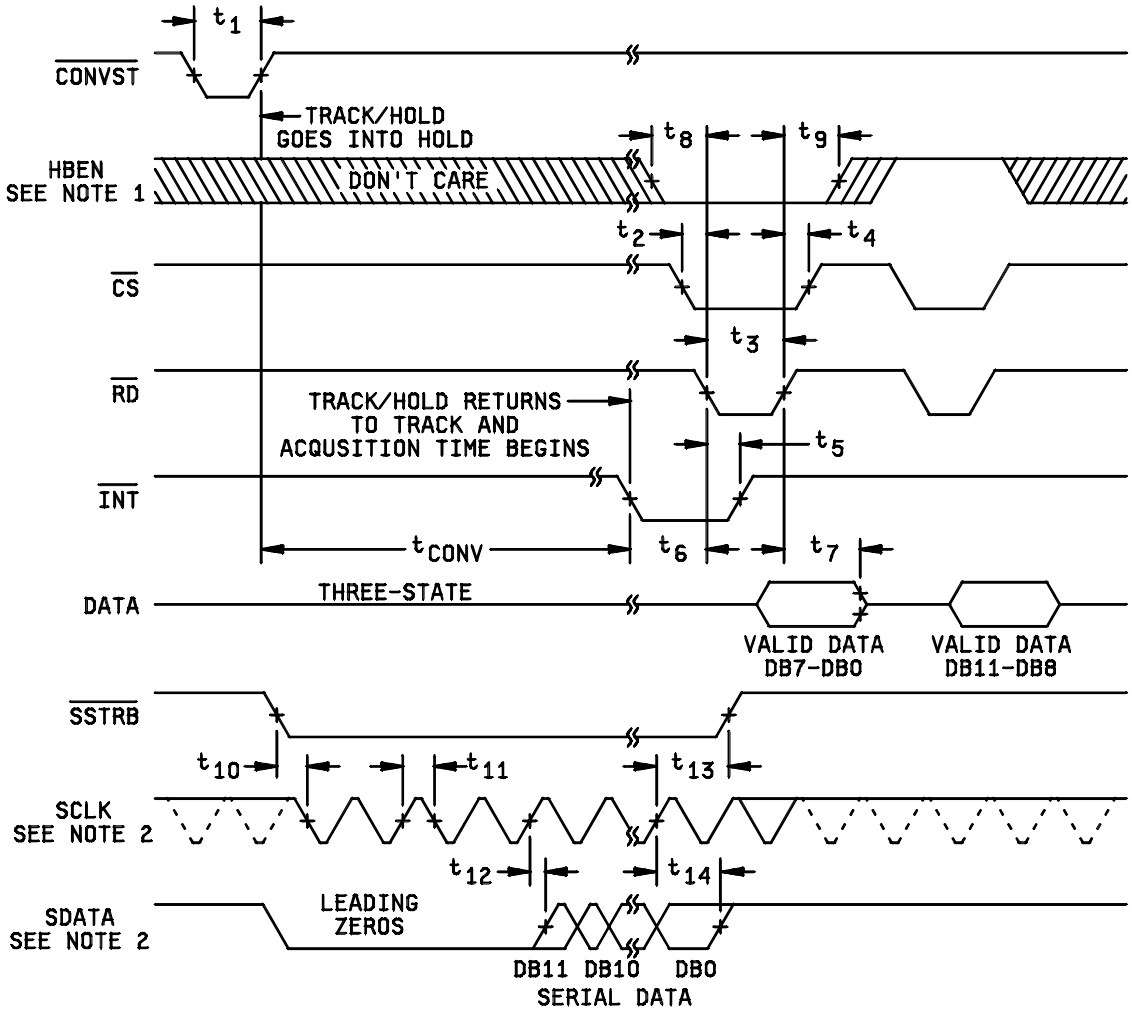


FIGURE 2. Timing waveforms.

Mode 1, byte or serial read



Notes:

1. Times t_2, t_3, t_4, t_8, and t_9 are the same for a high byte read as for a low byte read.
2. External 2 kΩ pull-up resistor.
3. External 2 kΩ pull-up resistor, continuous SCLK (dashed line) when 12/ $\overline{8}$ /CLK = -5.0 V, noncontinuous when 12/ $\overline{8}$ /CLK = 0 V.

FIGURE 2. Timing waveforms – Continued.

Mode 2, 12-bit parallel read

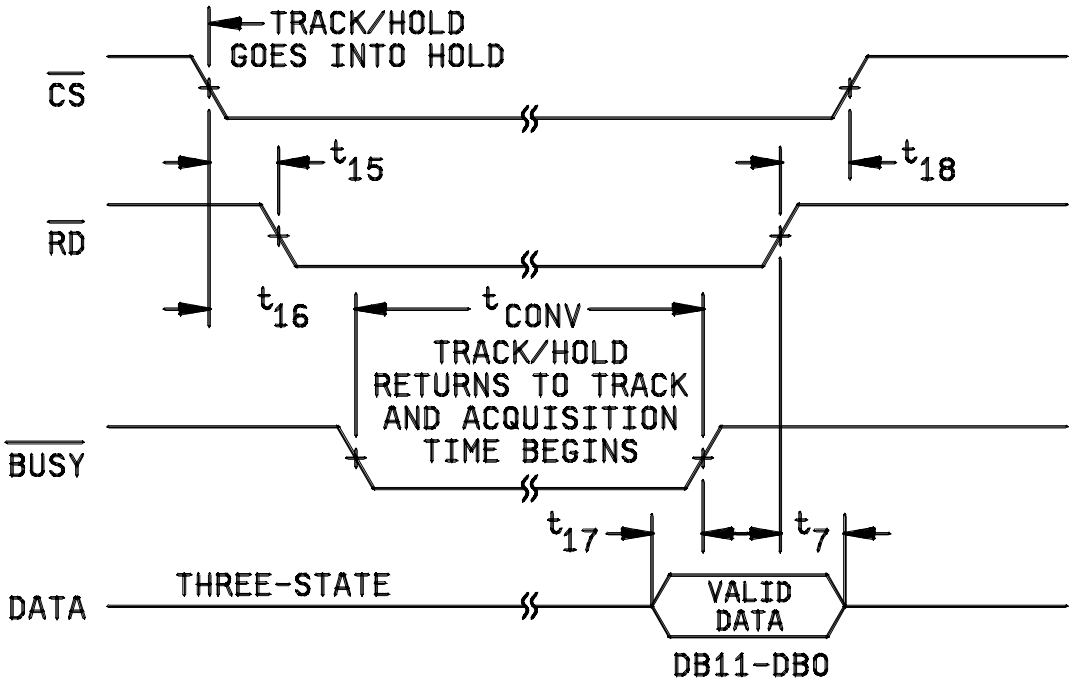
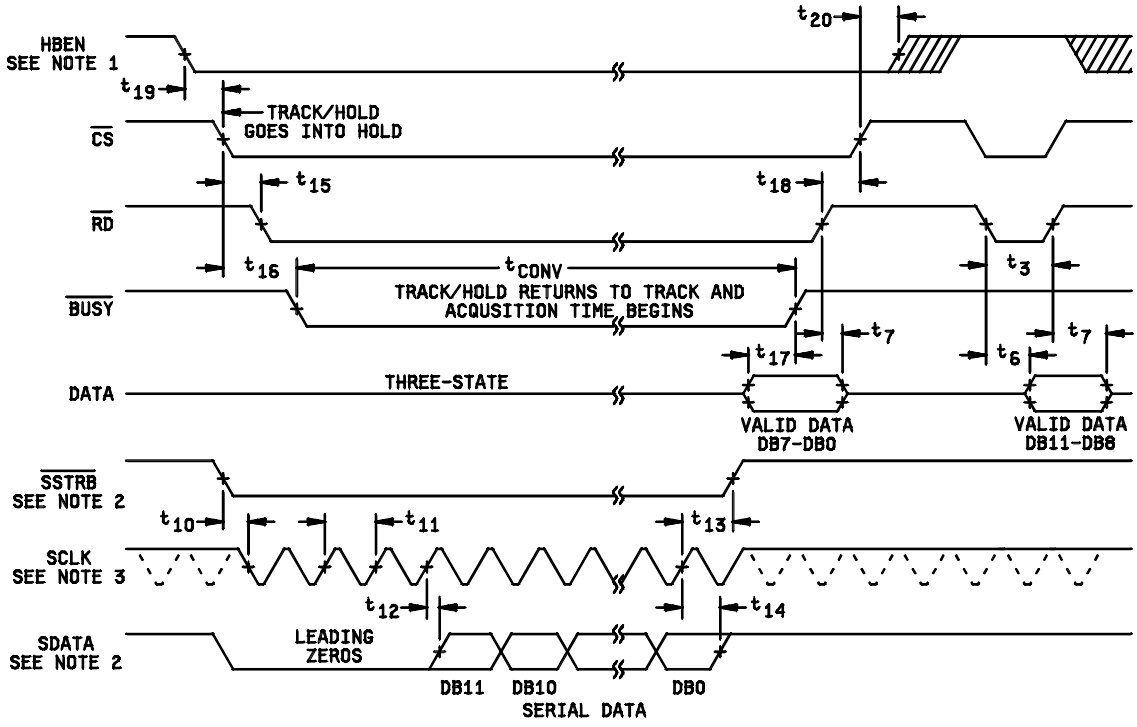


FIGURE 2. Timing waveforms – Continued.

Mode 2, byte or serial read



Notes:

1. Times t_2, t_3, t_4, t_8, and t_9 are the same for a high byte read as for a low byte read.
2. External 2 kΩ pull-up resistor.
3. External 2 kΩ pull-up resistor, continuous SCLK (dashed line) when 12/ $\overline{8}$ /CLK = -5.0 V, noncontinuous when 12/ $\overline{8}$ /CLK = 0 V.

FIGURE 2. Timing waveforms – Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, D, or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample of five devices with zero rejects shall be tested.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1,2,3,9,10,11 1/	1,2,3,9, 1/ 10,11	1,2,3,9, 1/ 10,11
Group A test requirements (see 4.4)	1,2,3,4,9,10,11	1,2,3,4,9, 10,11	1,2,3,4,9, 10,11
Group C end-point electrical parameters (see 4.4)	1	1	1,2,3,4,9, 10,11
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	----	----	----

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, D, or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-04-11

Approved sources of supply for SMD 5962-93179 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9317901MLA	24355	AD7876TQ/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Rt. 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of Contact: Bay F-1 Raheen Ind. Estate Limerick, Ireland